In the specification:

Page 1, lines 4 to 7, amend the paragraph to read as follows:

Embodiments of the present invention are related to commonly-assigned U.S. patent application, serial number 10/026,085 ~~—/——,——~~, filed December 21, 2001 ~~herewith~~ by Watts, entitled "Parallel Integrated Circuit Test Apparatus and Test Method," which is incorporated herein by reference.

Page 14, line 21 to page 22, line 4, amend the paragraph to read as follows:

In an embodiment of the invention wherein the first tester 336 in the apparatus 300 comprises a low cost tester and the second tester 308 comprises a high cost tester, preferably, the first tester 336 first test procedure is completed by the completion of the second tester 308 second test procedure. Preferably, there is no idle time on the high cost tester 308, to achieve maximum efficiency. In one embodiment, the test times for the first tester 336 and the second tester 308 are equal.

Page 16, lines 1 to 6, amend the paragraph to read as follows:

The IC's tested by the test apparatus 300 may be packaged. IC's packaged with a wide variety of types of IC packages may be tested with the test apparatus described herein, including IC packages such as quad flat packs, ball grid arrays, and pin-grid arrays, as examples. Alternatively, embodiments of the invention may be applicable for IC's on wafer, to be described further here. The apparatus may include a multiplexer ~~is~~ adapted to multiplex the first and second test procedures on the first and second IC's.

Page 20, lines 1 to 16, amend the paragraph to read as follows:

A block diagram of another embodiment of the present invention is shown in Figure 5. In this embodiment, the test apparatus 300 includes a plurality of testers

336/308/370, each being coupled to a single handler 304 via a corresponding test head 340/310/374, respectively. First tester 336 may comprise a low cost tester and the test apparatus 300 may not include an environmental chamber for IC's to be tested by the first tester 336 within the handler 304, for example. Second tester 308 and third tester 370 may comprise high cost testers, and the apparatus 300 may include an environmental chamber 361 for IC's under test by the second tester 308, and/or an environmental chamber 376 for IC's under test by the third tester 370. The environmental chambers 361/376 may be adapted to subject IC's to different environmental tests, e.g. the environment parameters of environmental chamber 361 may be different than the environmental parameters of environmental chamber 376. A plurality of other testers, not shown, may be included in the test apparatus 300. Sets of IC's may be tested with test procedures from the first, second and third testers 336/308/370 in parallel, or simultaneously, in accordance with this embodiment of the present invention.